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Review Article

DESIGN OF ONCHIP LOW DROPOUT REGULATOR FOR POWER MANAGEMENT APPLICATION

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ABSTRACT

A low dropout (LDO) regulator is proposed in this paper. The regulator is designed with classic five pack model to decrease the number of devices and make the design compact and also reduce the power consumption. The system is designed and simulated in cadence virtuoso environment under 180 nm technology node. Three models of LDO are proposed, in this paper, with all having same error amplifier but with small variations. The advantages and disadvantages of each model will be discussed in the paper. The LDOs have linear characteristic over a good input range. It has a good transient response to load variation.

Keywords: Low dropout, Analog driver, Transients.

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INTRODUCTION

With the trend of decreasing the device size and working with lower technology node, the need of portable power management system has become an essentially important in the digital world. As result linear regulators which are in the heart of the integrated power management system have gain considerable importance, providing an analog solution to power the digital chips. Low dropout (LDO) also finds its application in digital camera, LCD monitors, etc. The battery operated mobile devices needs a regulation free power supply in noise-sensitive environment. Here, an attempt is taken to design a power efficient LDO with low transient overshoot and undershoot under a given variation is load.

DESIGN ASPECTS AND OPERATING PRINCIPLE

Fig. 1 indicates a simple LDO regulator. In the further discussion, an introduction and working principle of LDO regulator are given along with the design challenges.

The basic concept of voltage regulators starts with the requirement of supply a constant voltage V_{OUT} in spite of the change in V_{DD}. This provides a means of regulating the voltage from the constant DC source and minimizes any fluctuation in the voltage during switching of load circuits. This needs a reference because it by itself will not hold the voltage accurately. The quiescent current of the device is maintained lower so that the current can be pushed into the load more and in turn which will increase the efficiency of the regulator.

$$n=\frac{P_{out}}{P_{in}}=\left(\frac{V_{OUT}}{V_{OUT}+V_{DROP}}\right)*\left(\frac{I_L}{I_L+I_Q}\right) \quad (1)$$

To make a good regulator, the value of V_{DROP} and I_Q must be small. P-type metal oxide semiconductor (PMOS) is used here to have a lower drop across the device hence the name justifies, low drop regulator. If allowed to get a higher drop then N-type metal oxide semiconductor (NMOS) could be used, which also have some advantage since the output resistance looking from the source is $1/g_m$ which will further be reduced by feedback. Voltage regulator has to provide a constant voltage output with a very low output resistance because essentially that is the principle topology behind a voltage controlled voltage source. Hence, the popular way to achieve the specification of low output resistance is a shunt feedback. This can give a feeling that it is somewhat like a voltage amplifier, but certain characteristics in the following articles will give us an intuitive understanding how it is unique from an amplifier. Furthermore, the output voltage is scaled version of the input (which will depend on the ratio of the resistor value used in resistance divider circuit) also try to achieve the upper voltage swing near to V_{DD} (though there will be some drop across the device). We are powering the circuits in the load. The reason the low drop out is specified is that given a particular V_{DD}, we would like the output to go as close to V_{DD} as possible. Other desirable characteristics are the output resistance should be as low as possible which is practically not possible since the incremental resistance will depend on the incremental change in V_{OUT} to that of change in load current and this gives a mathematical parameter to quantify load regulation. Moreover, the change in output to that of supply gives the line regulation. For a good regulator, these must be as small as possible. So with the change in V_{DD}, the V_{OUT} must not change and also if the load starts drawing abrupt current (step change during switching the load), the transient response should be smooth and must fluctuate less with respect to the desired value. This is the basic purpose of a regulator.

One more parameter, we should add to specification, i.e., power supply rejection ratio (PSRR) which is given by:

$$\frac{V_{OUT}}{V_{DD}}=\frac{1}{PSRR}<1 \quad (2)$$

Hence, it should be high. Earlier we talked about line regulation which is measured in DC. Same is done at higher frequencies and this is given by PSRR. So even if high regulation in V_{DD} is maintained at very high frequency that does not affect the V_{OUT}. The reason we are interested in different frequencies is because there are circuits like ring oscillators which are more sensitive to noise at particular frequencies.

DESIGN CHALLENGES

Given a V_{DD} and V_{OUT} specification, a PMOS transistor could be placed across it. Hence, the PMOS transistor needs to be driven by a controlled gate voltage. Hence, the resistive divider network gives the means of dividing the voltage and feeding back to an error amplifier. In addition, this error amplifier is going to have a reference as one input and this feedback resistance as other. This error amplifier will integrate the difference of voltage will drive the gate of the PMOS transistor. The gate-source capacitance is used to do the integration implicitly. The output

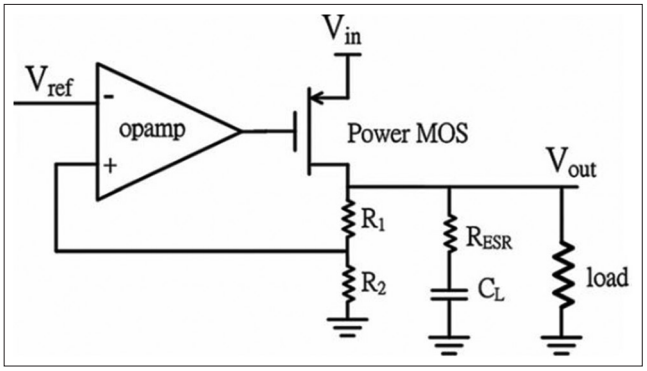

Fig. 1: Basic low dropout schematic

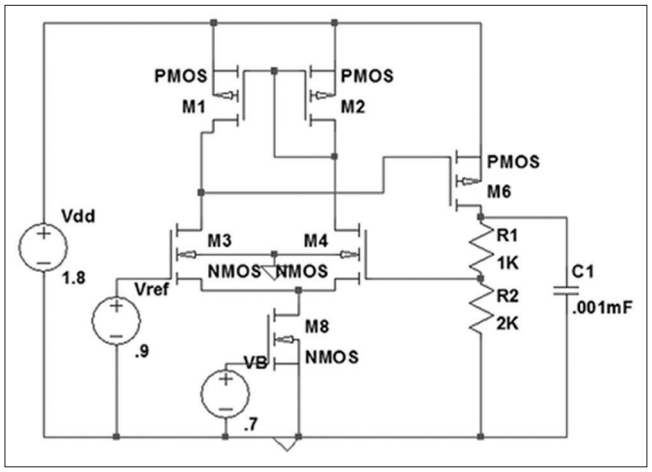

Fig. 2: Model 1 schematic

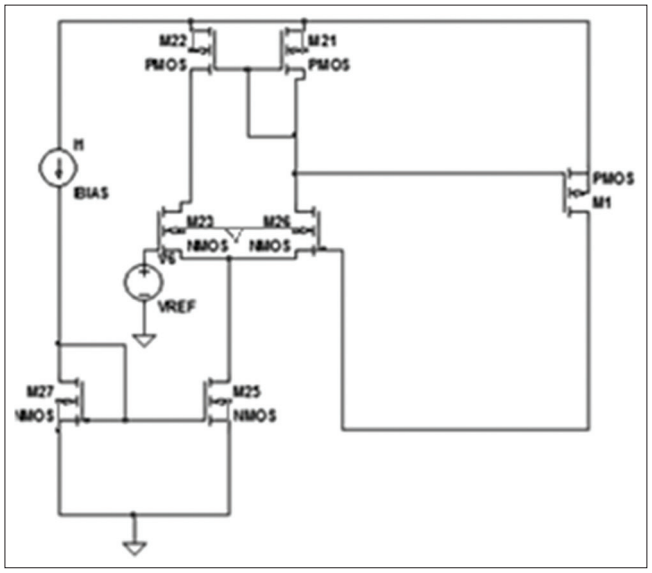

Fig. 3: Model 2 schematic

resistance is given by:

$$R_{OUT}=\frac{r_{ds0}}{1+A_0} \tag{3}$$

A_0 is the DC loop gain given by:

$$A_0= g_{m1}\, r_{01}\, g_{m0}\, r_{ds0}\frac{R_1}{R_1+R_2} \tag{4}$$

Where g_{m1} and r_{01} are of the error amplifier and g_{m0} and r_{ds0} is of PMOS. As A_0 is very large so the R_{OUT} will be very small. This is good but in case if load current has gone under a step change then r_{ds0} will increase g_{m0} will decrease making the condition worse. It happens like if the load current undergoes a step change then it takes some time for the gate voltage to change because the PMOS which is being used is a large device and hence the gate capacitor value is large which takes time to charge. And since, the quiescent current is required to be small so fast response cannot be expected. So on the instant of transient, the output voltage is expected to step down to a very less value. To avoid this, we place an output capacitor which will retain the voltage at the instant of transient till the feedback comes into action. What its turns out that for introducing this capacitor in the output made the regulator less stable since some poles and zeros will be introduced due to placing this capacitor which should be taken into account. Two dominant poles will be surely there: One due to load capacitance and another due to high gate capacitance. Other poles could be as well could be find inside the error amplifier as well. This gives some condition to be satisfied to make the regulator stable, and it turns out that this brings a constraint on output resistance r_{01} and which translates into limiting the DC gain considerably. So the condition is;

$$r_{01}<\frac{C_0}{C_{gs0}}g_{m1}g_{m0}\beta \tag{5}$$

And DC gain;

$$A_0=g_{m1}r_{01}g_{m0}r_{ds}\beta \tag{6}$$

But in reality, as high resistance is used in output, so R_{ESR} of the capacitance will be high as well to nullify the effect another small capacitor is introduced which limits the DC gain further.

$$r_{01}<\frac{C_0||C_{gs0}}{C_{gs0}}g_{m1}g_{m0}\beta \tag{7}$$

This further limits the DC load regulation.

LDO SCHEMATIC DESIGNS

LDO regulators are designed in three topologies, each having its own advantages and disadvantages. Each one will be discussed one by one. In the later section when the simulation results will confirm the same.

In all the designs, the classic five pack model is used for designing the error amplifier. This essentially decreases the number of devices which makes the integration easy. This is used for driving the digital circuit, so it is very important to bring the regulator in compact form and reduce the size as much as possible.

All the three models are presented along with its schematics, and the advantages are discussed in brief. The third model is actually an extension of the second model where we introduce an additional analog driver. The advantage of all the topologies will be discussed in the following sections along with the supporting simulation results. The ultimate aim is to make a robust design where the voltage is kept constant at a desired level for large range of load (tera ohm to femto ohm) and maintain mA current level.

Among the three designs, the first design is very simple which is popularly used but the problem with the circuit is, as it is very difficult to realize very high resistance in integrated circuit (IC) so the current

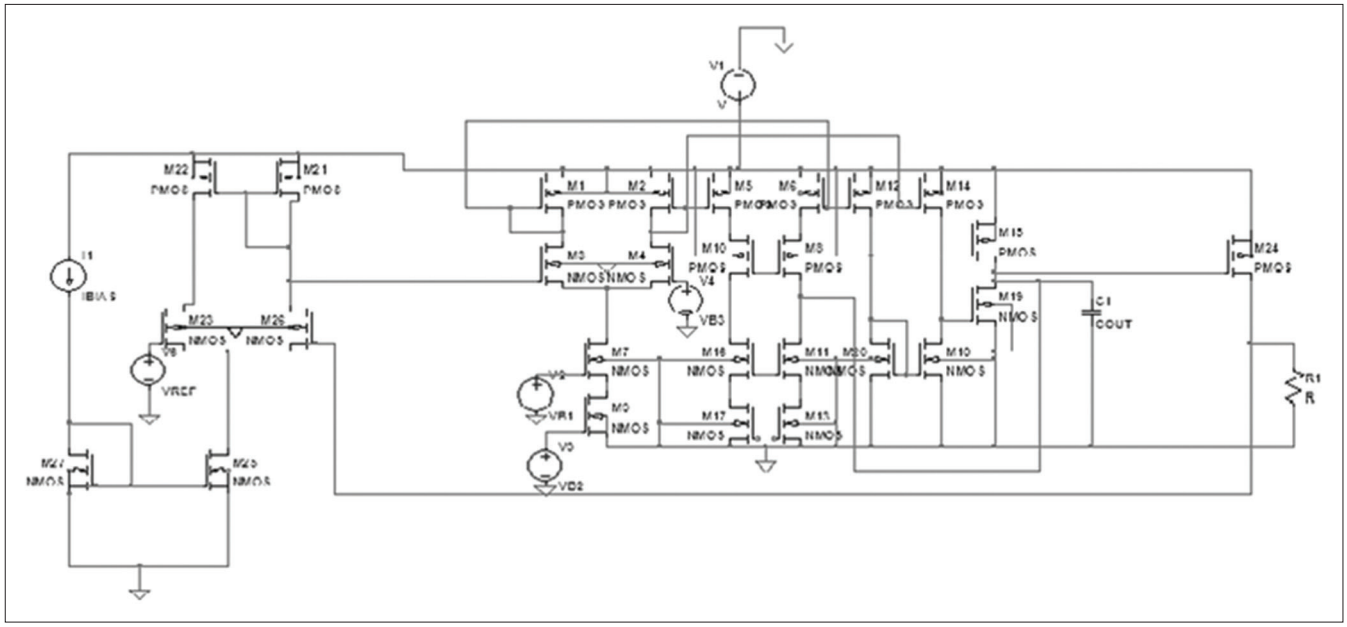

Fig. 4: Model 3 schematic

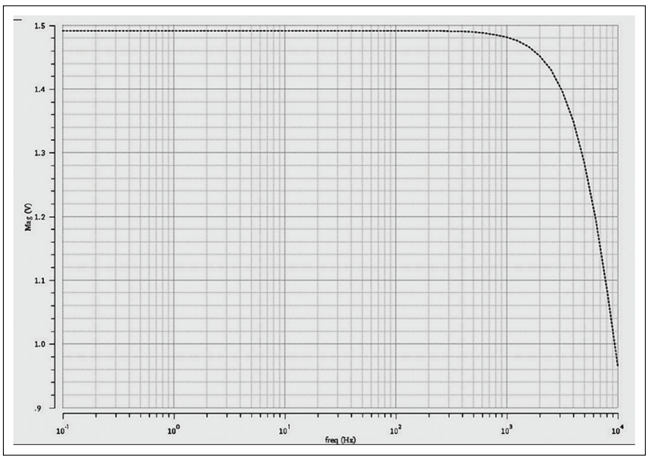

Fig. 5: AC response of Model 1

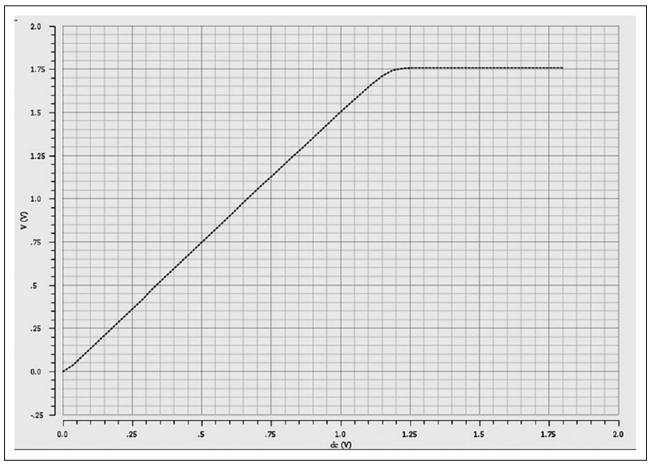

Fig. 7: DC characteristics of Model 1

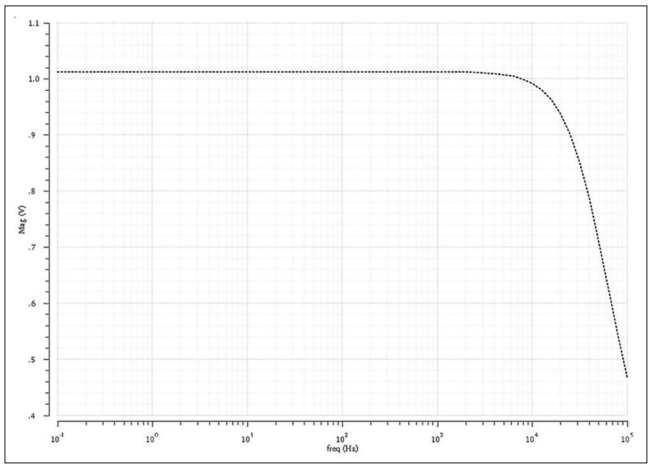

Fig. 6: AC characteristics of Model 2

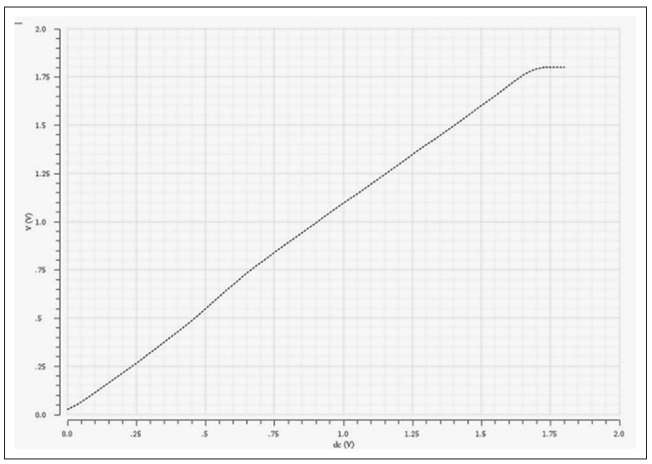

Fig. 8: DC characteristics of Model 2

through the resistance divider circuit is finite, making the output current very less.

In the second design instead of giving feedback from resistance divider, direct output is given to the gate of NMOS. Now since gate is high

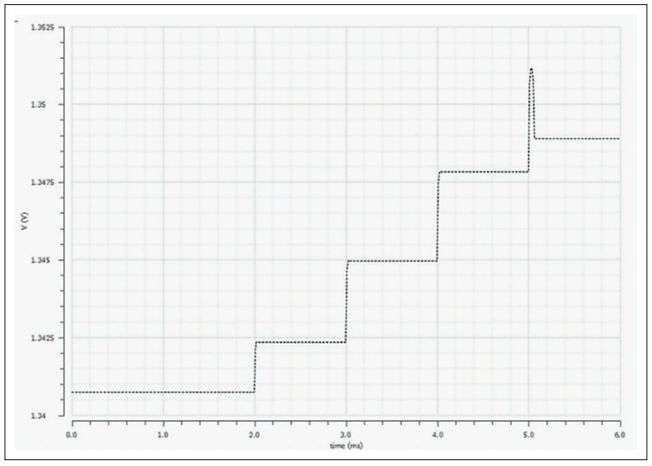

Fig. 9: Voltage transient characteristics of Model 1 low dropout regulator

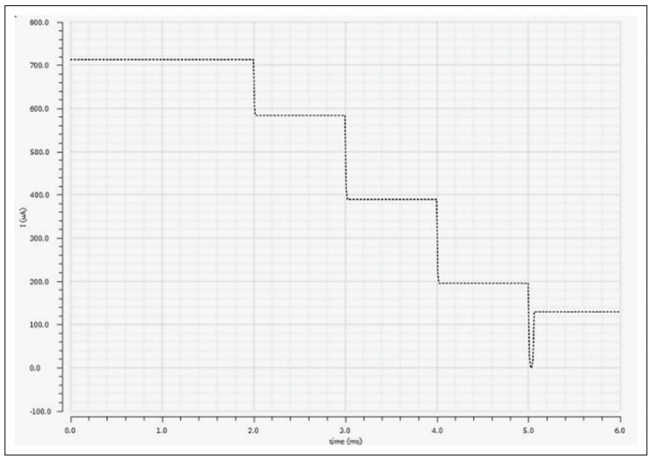

Fig. 10: Current transient characteristics of Model 1 low dropout regulator

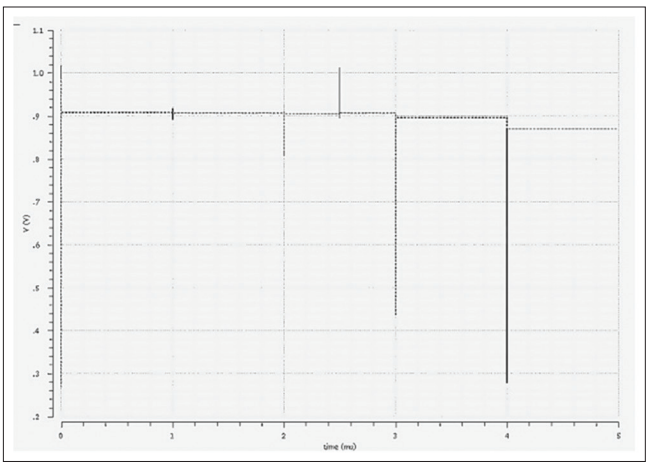

Fig. 11: Voltage transient characteristics of Model 2 low dropout regulator

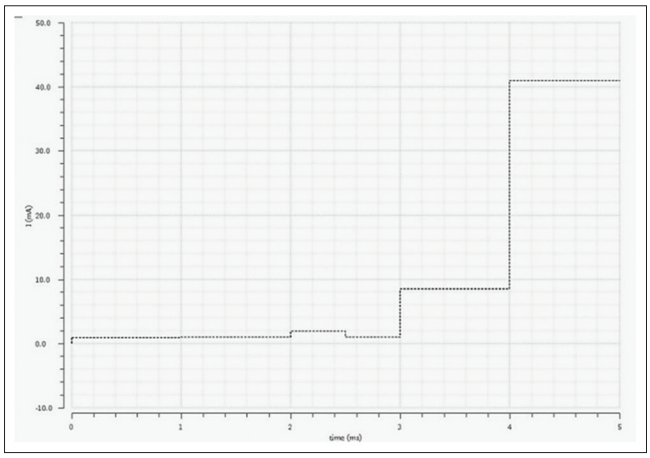

Fig. 12: Current transient characteristics of Model 2 low dropout regulator

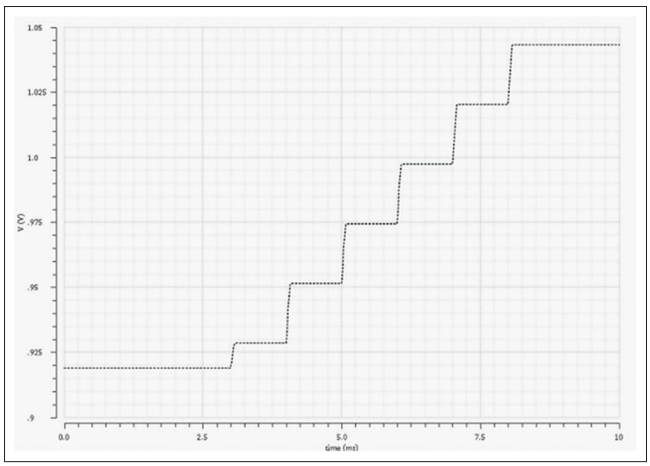

Fig. 13: Voltage transient characteristics of Model 3 low dropout regulator

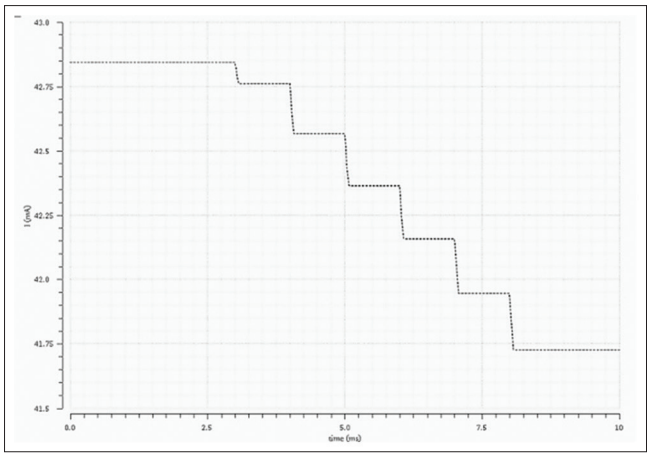

Fig. 14: Current transient characteristics of Model 3 low dropout regulator

resistance and ideally do not consume any current so all the current is pushed to load. But disadvantage of the circuit is that the voltage transients are very sharp.

Hence, we can see to get the transient response better we need to trade off in terms of output current.

Now to break this trade-off an additional analog driver is introduced between error amplifier and power MOS. The transient response has improved sharply as well as more current (mA order) current can be passed.

Introducing the analog driver has some other advantages as well. In the first design though large change in load does not affect the voltage much

but current is affected highly. Similarly, the second model is designed for fixed range of resistance (10 ohm-100 Kohm) after that the voltage starts degrading. The third model is only can be called universal for any load variation. For 1 femto ohm-1 tera ohm load, the circuit is simulated and produced as results. In the following article, the description of analog driver is given which is useful to understand its operation and how it is improving the overall load transient effect of the regulator.

ANALOG DRIVER DESIGN

In LDO, the large gate capacitance of power MOS degrades the bandwidth and hence the slew rate at the gate drive of the power MOS. This effect the load transient response of the regulator. It can be improved by paying the cost of higher quiescent current which again increase the static power consumption. Both the parameters cannot be improved with the generic topology of LDO. To achieve this, we introduce the analog driver between the core amplifier and the power MOS. So basically, the analog driver is designed to improve the load transient of the regulator. The output resistance of the analog driver is reduced by the unity gain feedback configuration. The dominant pole which occur at the gate of power MOS is shifted to higher frequency so the loop gain bandwidth of the LDO is improved. The load transient response of LDO which was limited by the slew rate at the gate drive of power MOS is now improved by the introduction of the analog driver. The driver provide current to charge and discharge the gate capacitance of the power MOS during load transition. In steady state, it is turned off. Although the quiescent current through driver is quite low, still it improves the slew rate at the gate drive. Hence, the load transient response is enhanced.

Normally, the driver act as a plug in module which is cascaded to the core amplifier. The analog driver implemented with current mirror amplified and current sensing circuit and which provide sufficient dynamic current to drive the gate of power MOS during load transition and shut off in steady state.

A systematic approach should be taken in designing the response time of the driving circuit and aspect ratio of the drive transistor to support the dynamic current to the drive the power MOS to ultimately achieve better transient response.

SIMULATION RESULTS

AC characteristics

As we can see the output is maintained at 1.5 V for high range of frequency (above 1 KHz).

The output is getting constant up to 10 KHz which is more from the Model 1.

DC characteristics

The input–output relation is linear as expected from a linear regulator and the linear up to 1.75 V. It is getting saturated due to the fact that resistor ratio allows that much variation.

We get linear characteristics in this model above 1.75 V which is making the system linear for higher range.

Regulation characteristics

In Model 1 transient characteristic of both voltage and current, the sudden spikes are very less and the variation in voltage level is also allowable. The only problem with such structure is that since a resistance divider circuit is present, so a large amount of current drained through it and that makes the output current very less.

In Model 2 to avoid the above problem, the resistance divider network is avoided rather direct output is given to the gate of NMOS which makes the whole current push through the load. Hence, the simulation shows that mA current could be pushed through the load but transient is high.

Another disadvantage of the structure is that it is limited to a load range. For our case, it is 10 ohm-100 Kohm.

However, the structure is very good since the output current that can be pushed is high. Now the challenge is to introduce something that will decrease the transient peaks and increase the load range without affecting the current. Hence, an analog driver is used after the error amplifier to serve the purpose. Now taking the advantage of this structure the third model developed. We now introduce the analog driver whose description is given above. That will help the load transient to get reduced which is also noticeable from the simulation results to follow. The analog driver is actually a voltage buffer and a current mirror amplifier which provide the dynamic current to drive the gate of the power MOS and remain shut off at steady state hence reducing the quiescent current consumption and static power loss.

In Model 3 with the implementation of the analog driver in the subsequent stage the voltage transients have decreased and also high mA current could also be pushed across the load.

This also increases the load range. Simulation is done from 1 femto ohm to 1 tera ohm and voltage and current variation became very less.

INFERENCE

Model 1 was designed as a simple regulator to maintain the voltage at a certain level fixed. It was doing but current that was pushed was getting drained out by the resistance divider. To decrease that direct feedback is given to gate of MOS which helped the current to be in mA level. However, the disadvantage was that the voltage transients we sharp for low resistance value. To avoid that analog driver is introduced in cascade to the error amplifier which improved the transient response.

CONCLUSION

In this paper, we present a simple design of LDO regulator designed in 180 nm technology node in Cadence Virtuoso environment. It gives a high bandwidth, good linear response with respect to input and expected transient response. The inclusion of analog driver further made the model better in terms of both transient response as well as current output. And since the error amplifier, we used is a simple five pack model which reduced the chip area and so it's easy to implement this on chip for powering digital ICs.

REFERENCES

1. Huang CH, Ma YT, Liao WC. Design of a low-voltage low-dropout regulator. IEEE Trans Very Large Scale Integr VLSI Syst 2014;22(6):1308-1313.
2. Lee H, Mok PK, Leung KN. Design of low-power analog drivers based on slew-rate enhancement circuits for CMOS low-dropout regulators. IEEE Trans Circ Syst II 2005;52(9):563-7.
3. Oh W, Bakkaloglu B. A CMOS low-dropout regulator with current-mode feedback buffer amplifier. IEEE Trans Circ Syst II 2007;54(10):922-6.
4. Lu Y, Wang Y, Pan Q, Ki WH, Yue CP. A fully-integrated low-dropout regulator with full-spectrum power supply rejection. IEEE Trans Circ Syst I 2015;62(3):707-16.
5. Giustolisi G, Palumbo G, Spitale E. Robust miller compensation with current amplifiers applied to LDO voltage regulators. IEEE Trans Circ Syst I 2012;59(9):1880-93.